

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Dmitriy Rumynin et al. Examiner: David H. Malzahn
Serial No.: 09/917,257 Group Art Unit: 2193
Filed: July 27, 2001 Docket: 1365.051US1
Title: A PARALLEL COUNTER AND A LOGIC CIRCUIT FOR PERFORMING
MULTIPLICATION

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(c)(2), Applicants hereby authorize the Commissoner to charge the fee of \$180.00 as set forth in 37 C.F.R. §1.17(p), to Deposit Account No. 19-0743. Please charge any additional fees or credit any overpayment to Deposit Account No. 19-0743.

Pursuant to 37 C.F.R. 1.98(a)(2), Applicant believes that copies of cited U.S. Patents and Published Applications are no longer required to be provided to the Office. Notification of this change was provided in the United States Patent and Trademark Office OG Notices dated October 12, 2004. Thus, Applicant has not included copies of any US Patents or Published Applications cited with this submission. Should the Office require copies to be provided, Applicant respectfully requests that notice of such requirement be directed to Applicant's below-signed representative. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

DMITRIY RUMYNIN ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date

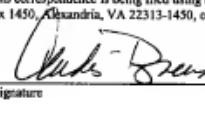
30 March '06


Timothy B. Cline
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 30 day of March, 2006.

Name

CANDIS BUENDING


Signature

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Under the Paperwork Reduction Act of 1995, no person is required to respond to a collection of information unless it contains a valid OMB control number.

Complete if Known Application Number 09/917,257 Filing Date July 27, 2001 First Named Inventor Rumynin, Dmitry Group Art Unit 2193 Examiner Name Malzahn, David			
		Sheet 1 of 1	
		Attorney Docket No: 1365.051US1	

US PATENT DOCUMENTS

Examiner Initials*	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date if Appropriate
	US-6,883,011	04/19/2005	Rumynin, D. , et al.	01/25/2001

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T ²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issus number(s), publisher, city and/or country where published.	T ²
		"Communication Pursuant to Article 96(2) EPC, for application No. EP 02 722 402.1, date mailed June 6, 2005", 3 Pages	
		SONG, PAUL J., et al., "Circuit and Architecture Trade-offs for High-Speed Multiplication", IEEE Journal of Solid-State Circuits, Vol. 26, No. 9, (September 1991),1184-1198	

EXAMINER**DATE CONSIDERED**